Jet Propulsion Laboratory
California Institute of Technology

Effect of radiation, endurance on pulsed programming

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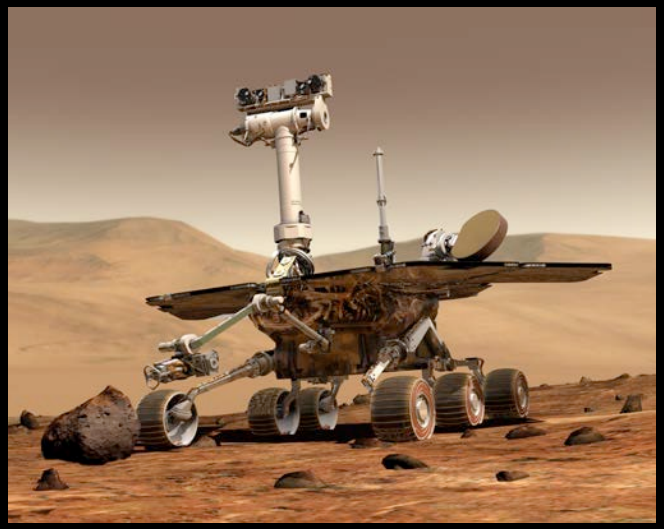
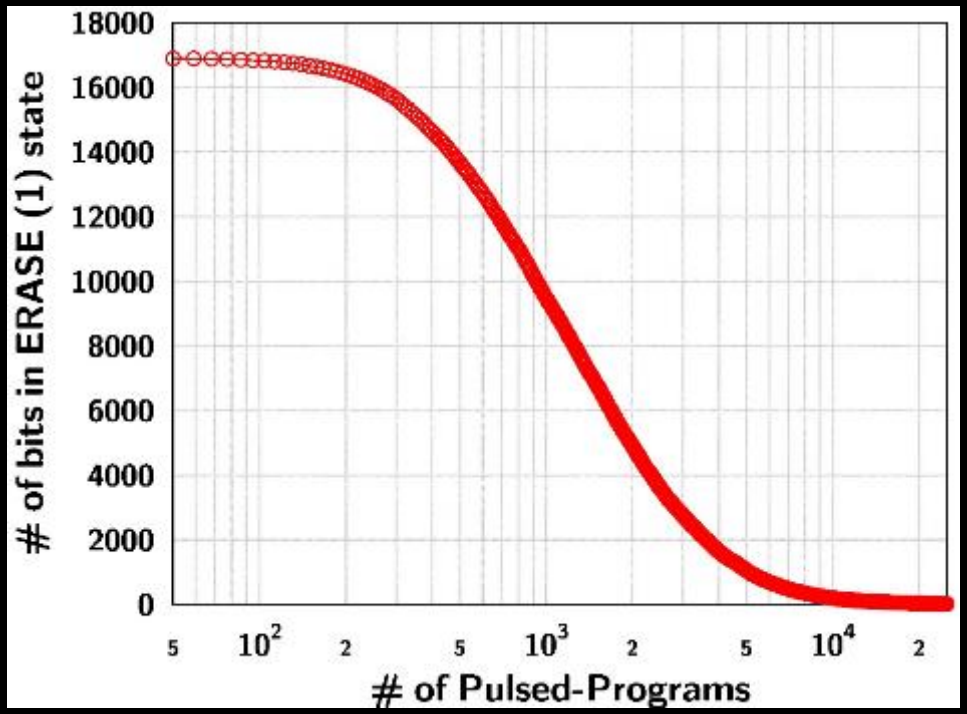
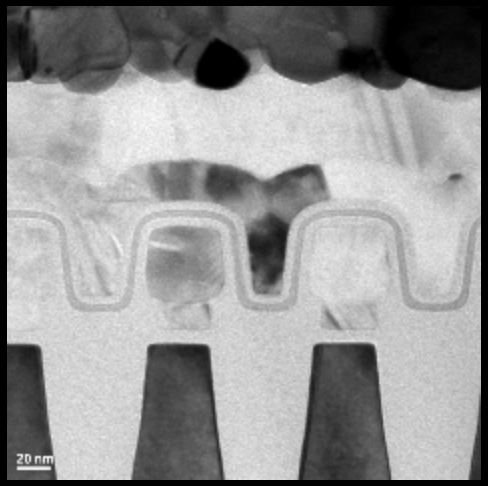
Presented by Avyaya J. Narasimham, Caltech Postdoctoral researcher

Our approach…



Pulsed Program Method





OUTLINE

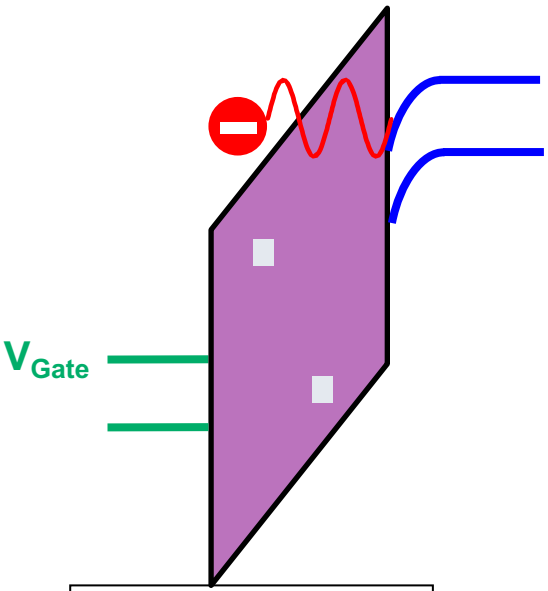
- Nature of traps: Endurance and Radiation
- Experimental setup
- Pulsed Programming and Pulse width
- Endurance, Radiation and Pulsed programming
- Coupled effect
- Conclusion and future work

INTRODUCTION

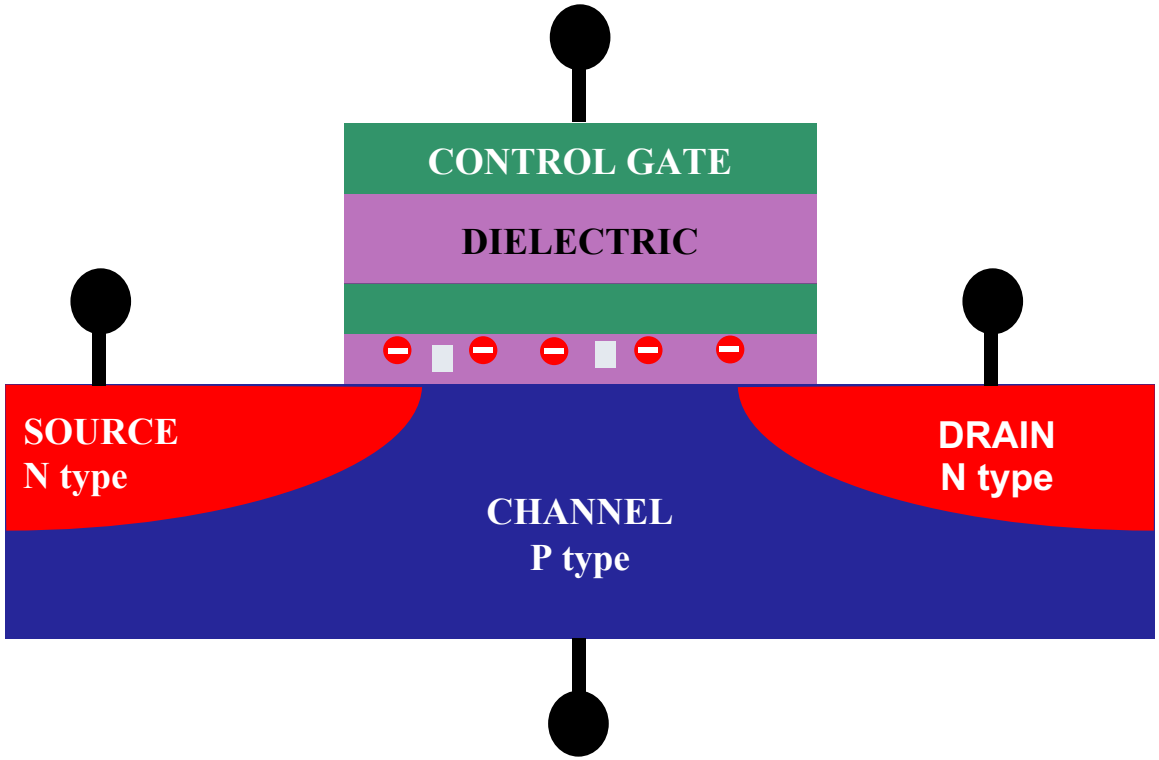
Nature of traps: Endurance

Programs-Erase stress traps electrons creating negatively charge traps

Fowler -Nordheim tunneling

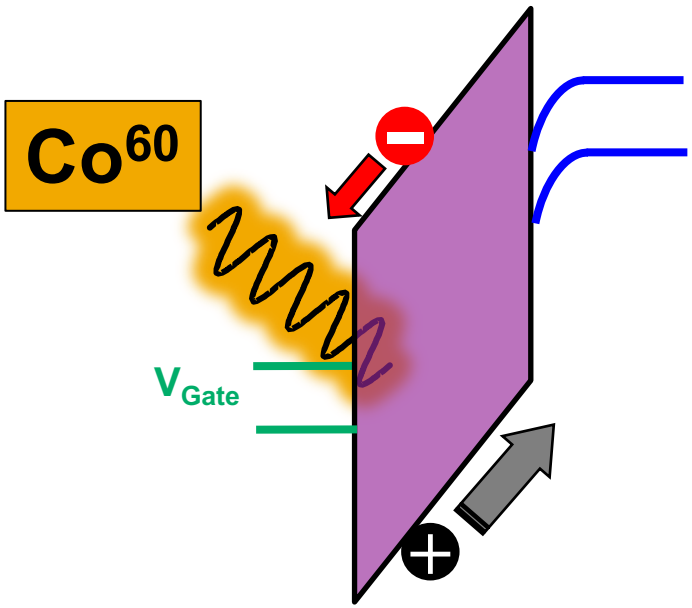


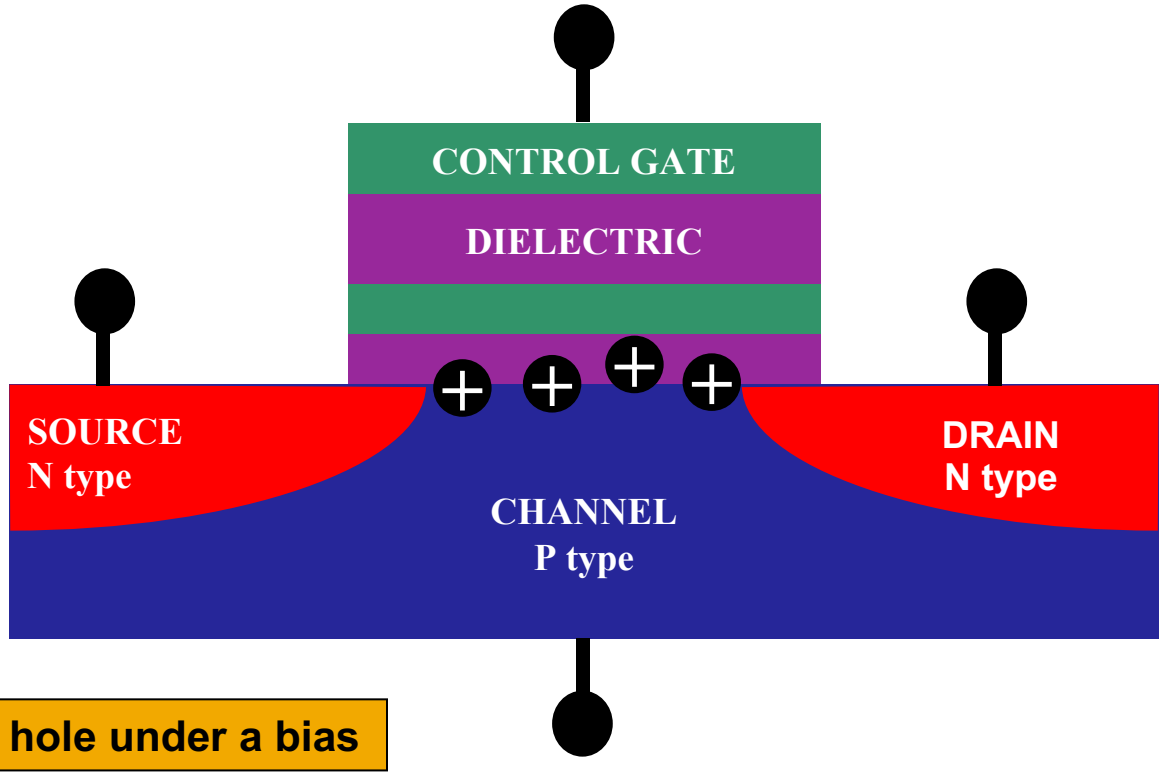
High electric field



Nature of traps: γ-Radiation

Incoming radiation creates electron-hole pairs and induces a hole-traps which are positively charged traps



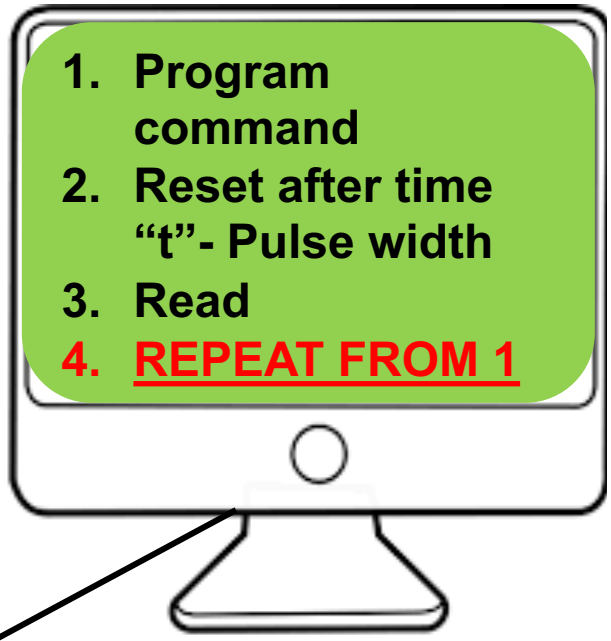


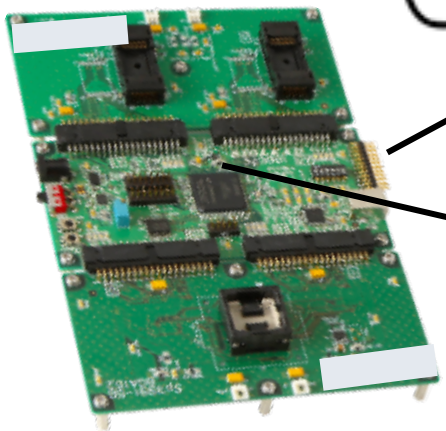
Electron is swept away faster than hole under a bias

EXPERIMENTAL SETUP

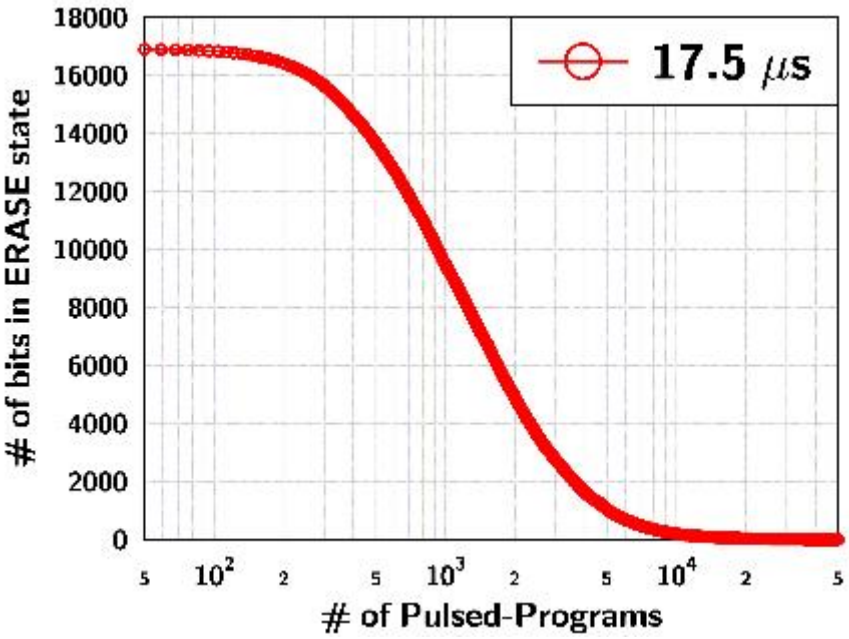
EXPERIMENTAL SETUP

Micron Technology Inc.



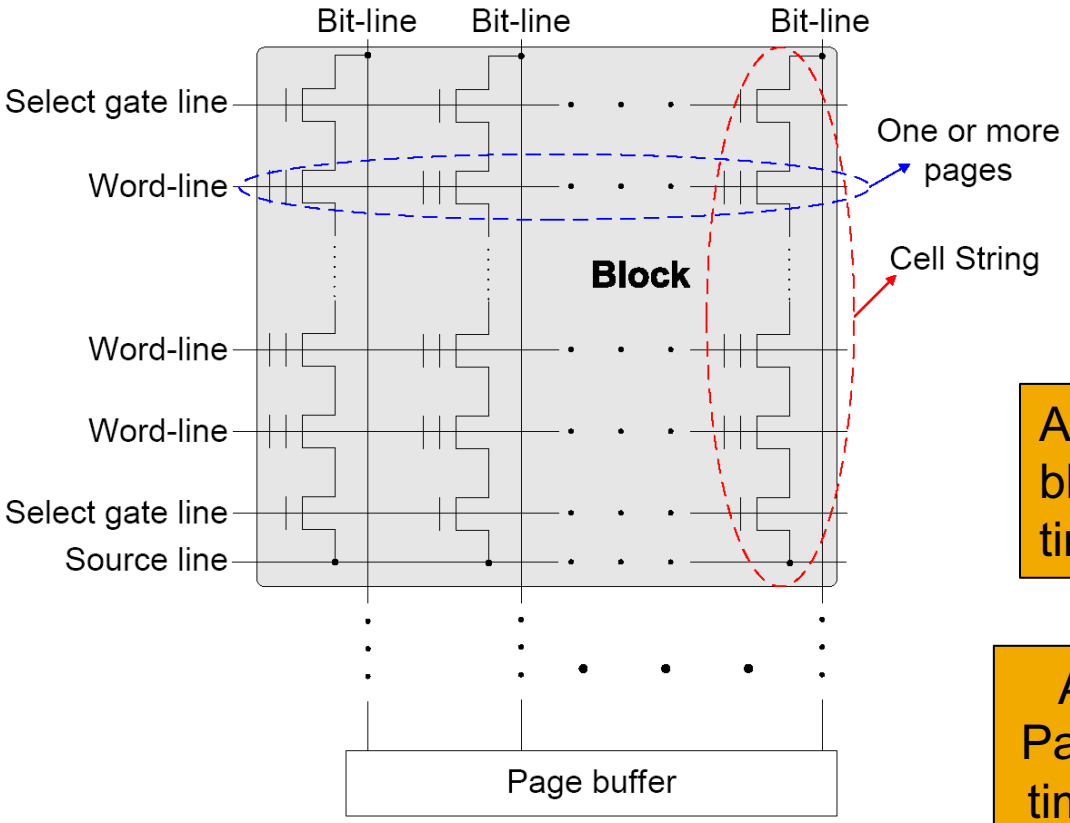


FPGA chip controls the NAND Flash.



The resolution of pulse width is limited by the FPGA, which is 50 ns

NAND Flash memory structure: Erase and Program operation



ARRAY

BLOCK

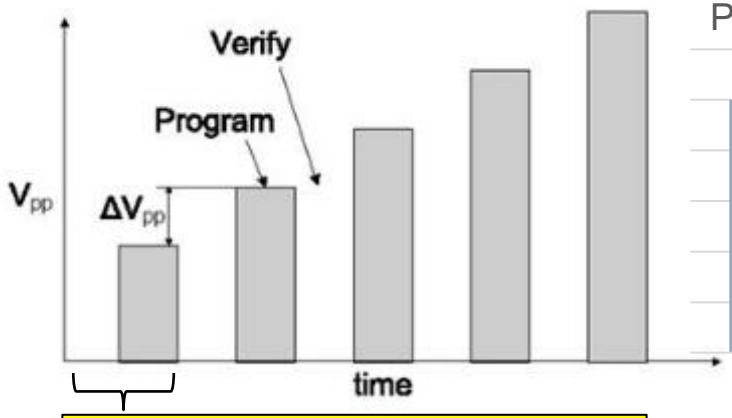
PAGE

A page contains 512 bytes to 8 K bytes

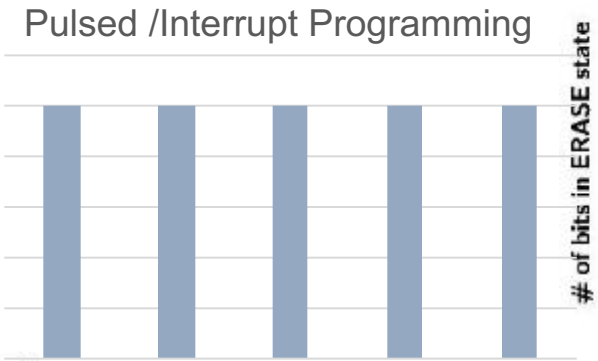
All the memory bits in the same block are erased at the same time in a single erase operation

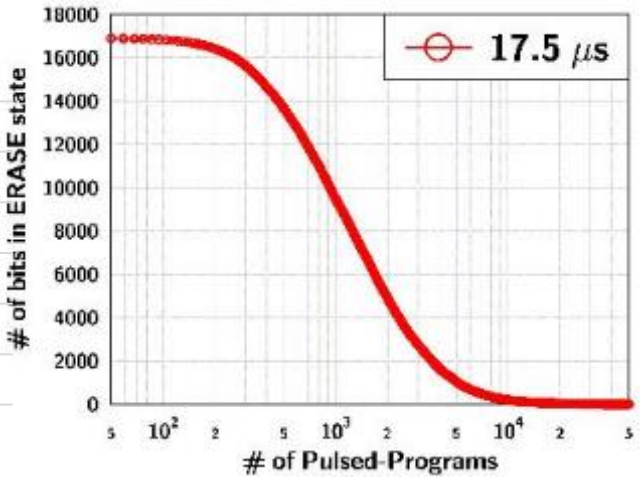
All the memory bits in the same Page are programmed at the same time in a single Program operation

Pulsed Programming and Pulse width



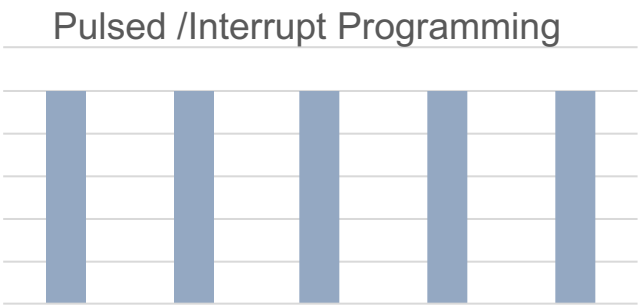
On the order of 10-50us



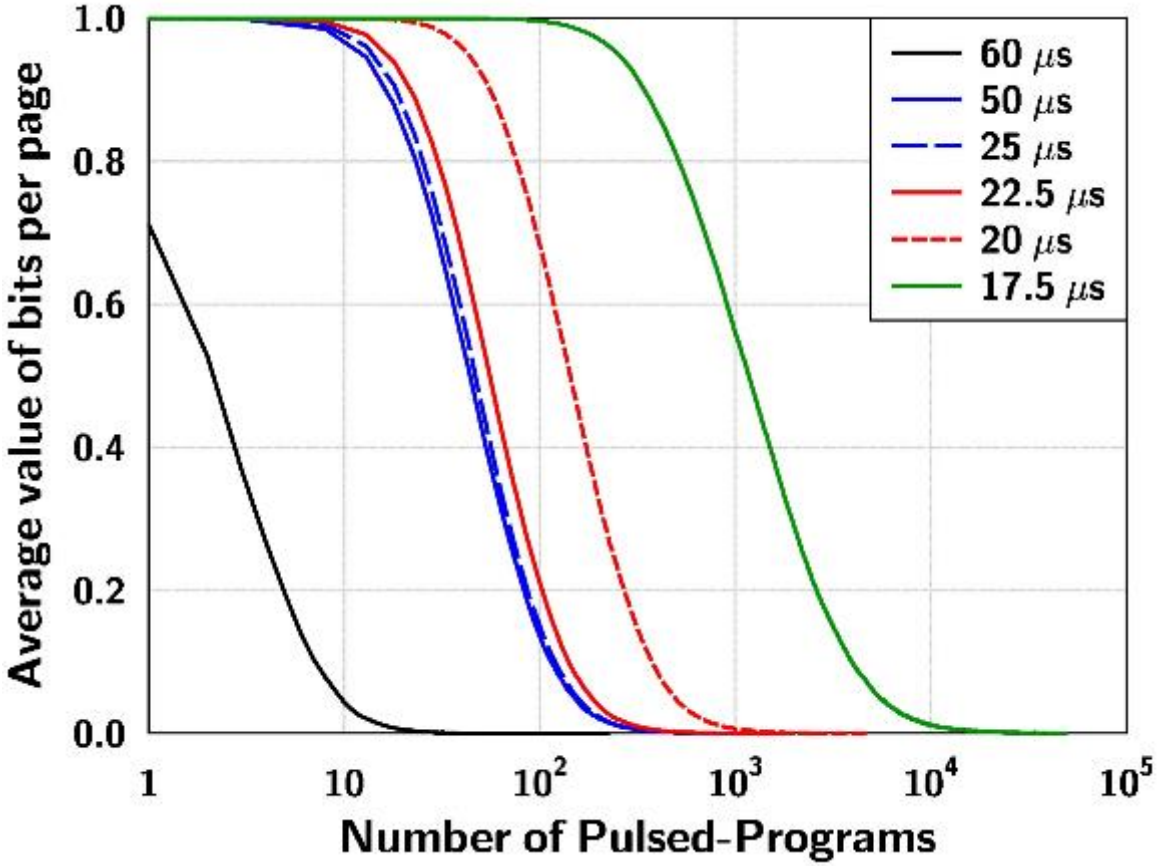


- Standard on chip programming uses a voltage ramp for successive pulses (left plot) taking ~220us to complete
- In our pulsed programming, we interrupt the on chip program command after ~20us so the expected program voltage is approx. constant (middle plot)
- Thus the number of pulses here would be significantly higher than on chip program pulses due to lake of voltage ramp (right plot)

Pulsed Programming and Pulse width

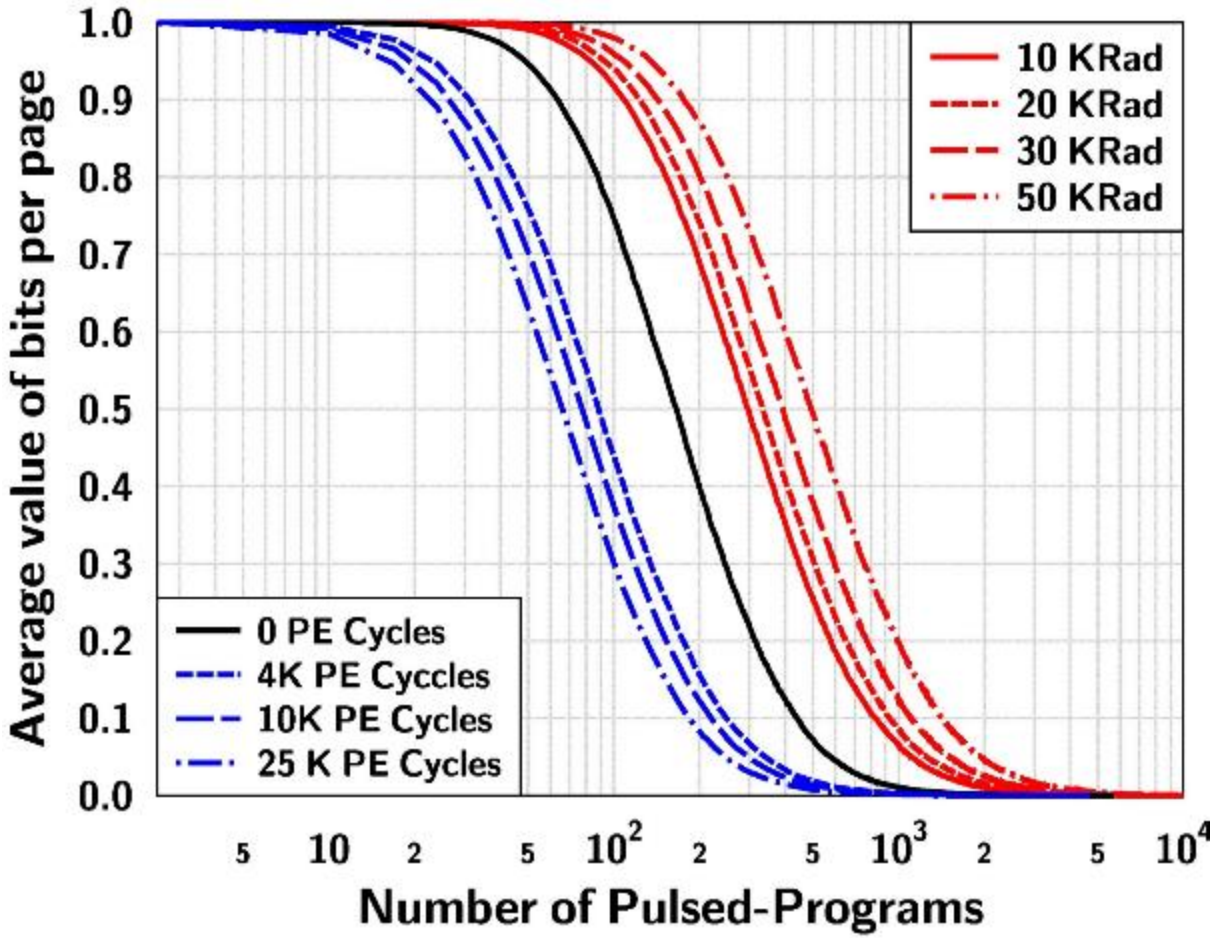


A longer pulse-width can program a larger population of bits on a page. Repeating the pulse program operation many times will eventually program the entire page

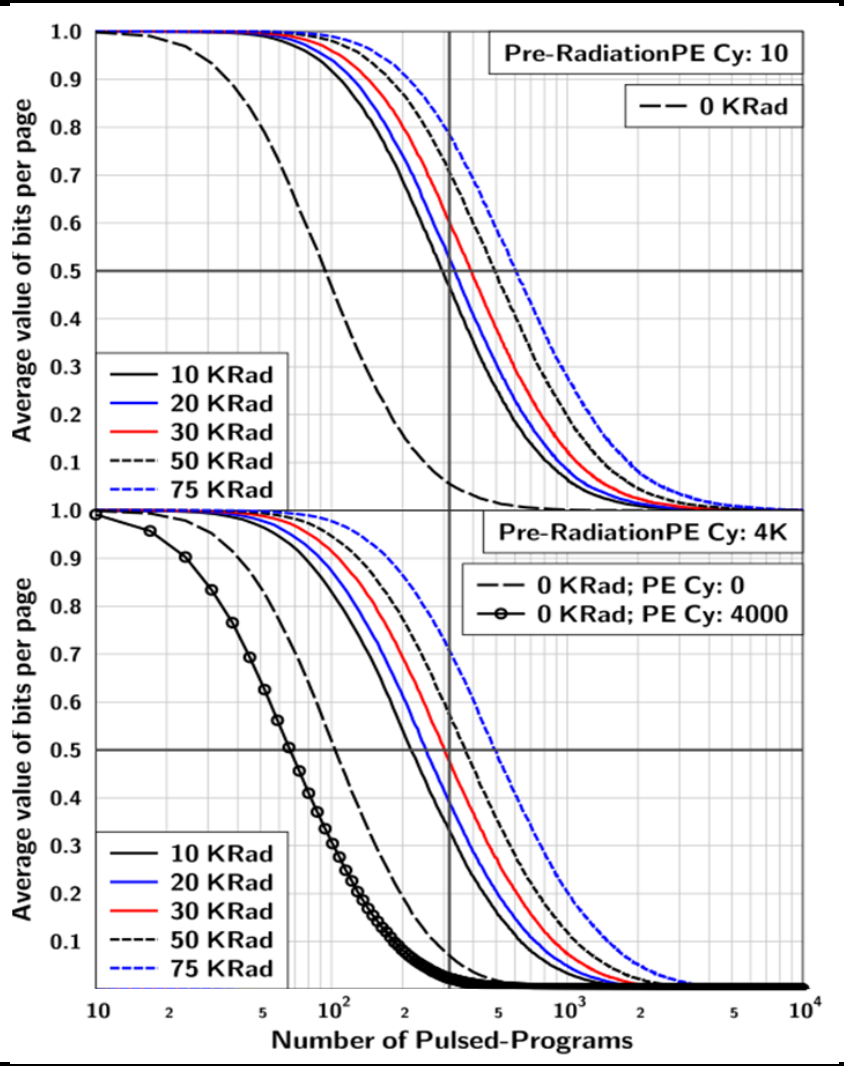


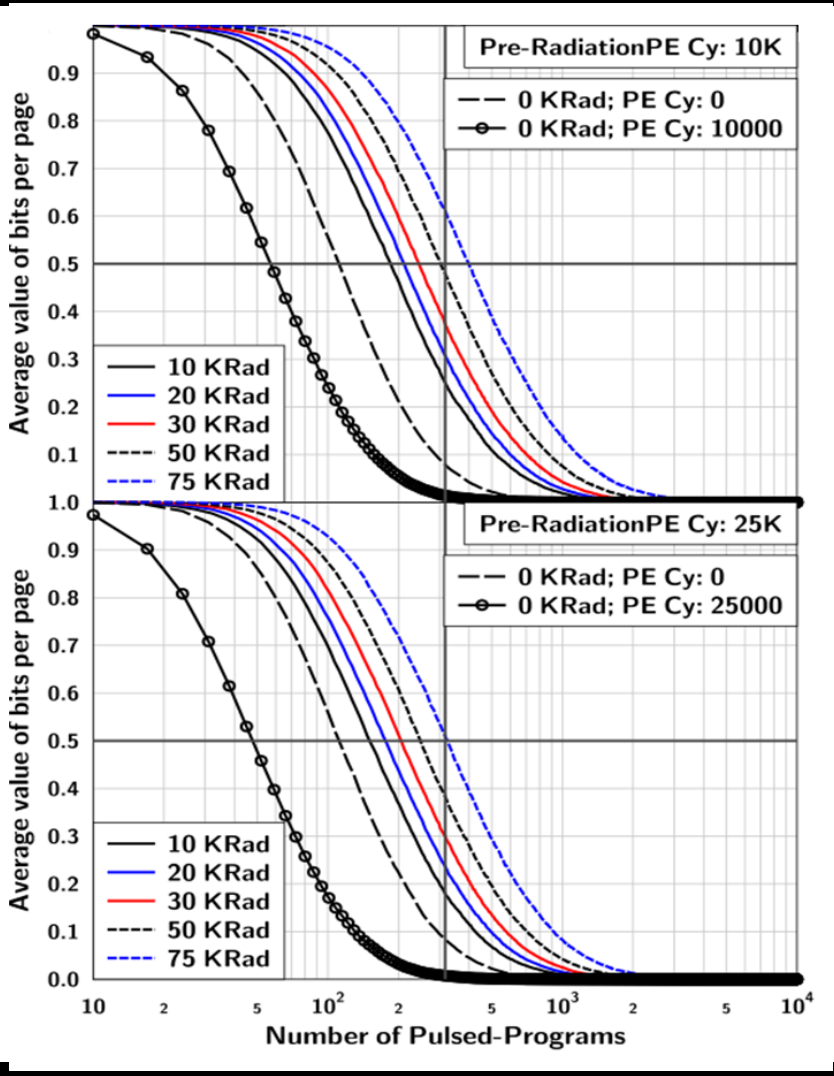
Opposing effects of radiation and endurance

Radiation exposure made the bit cells on the page more difficult to program, while Program-erase stress made the bit cells on the page easier to program



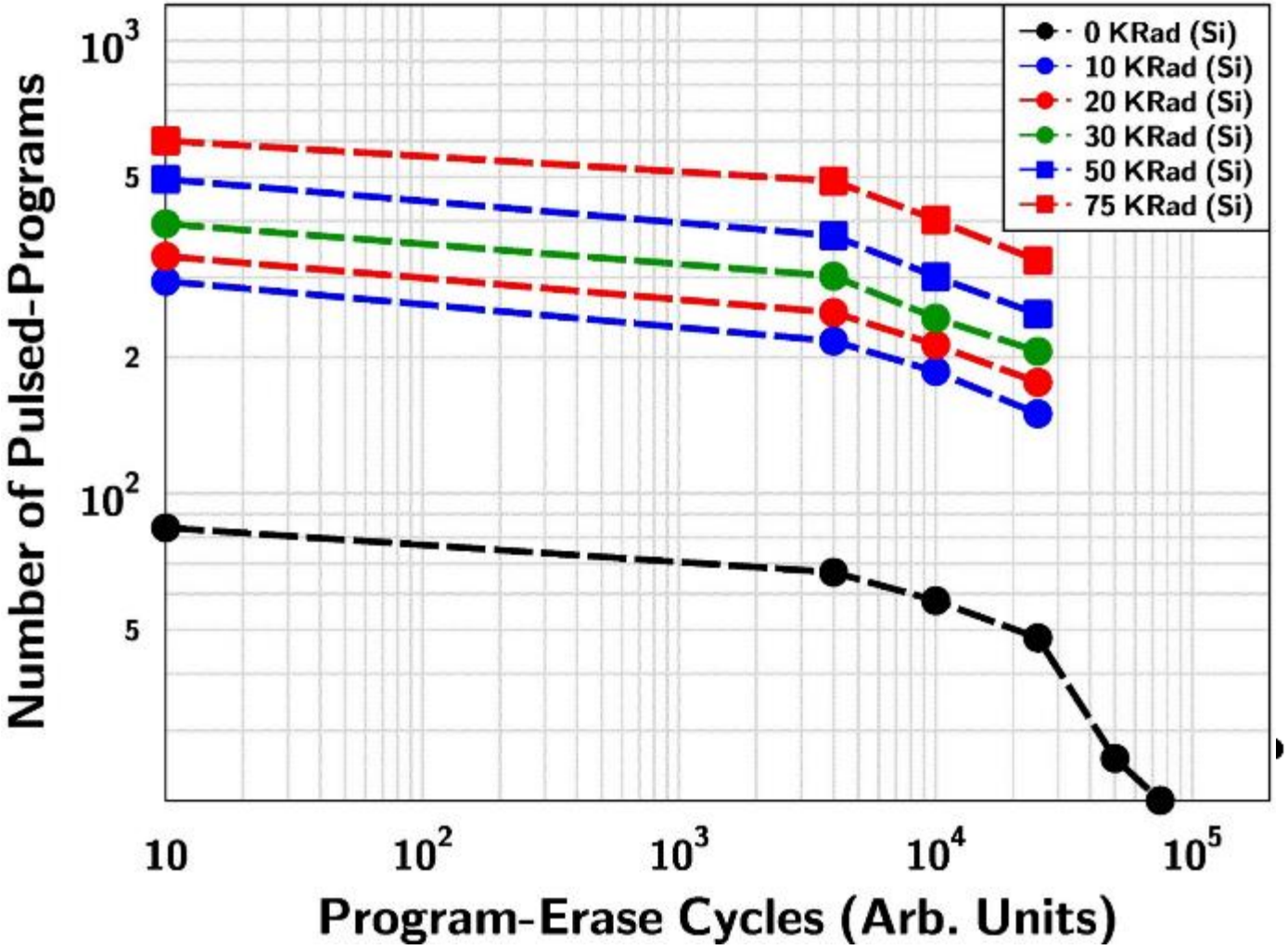
Coupled effect of Radiation and Endurance



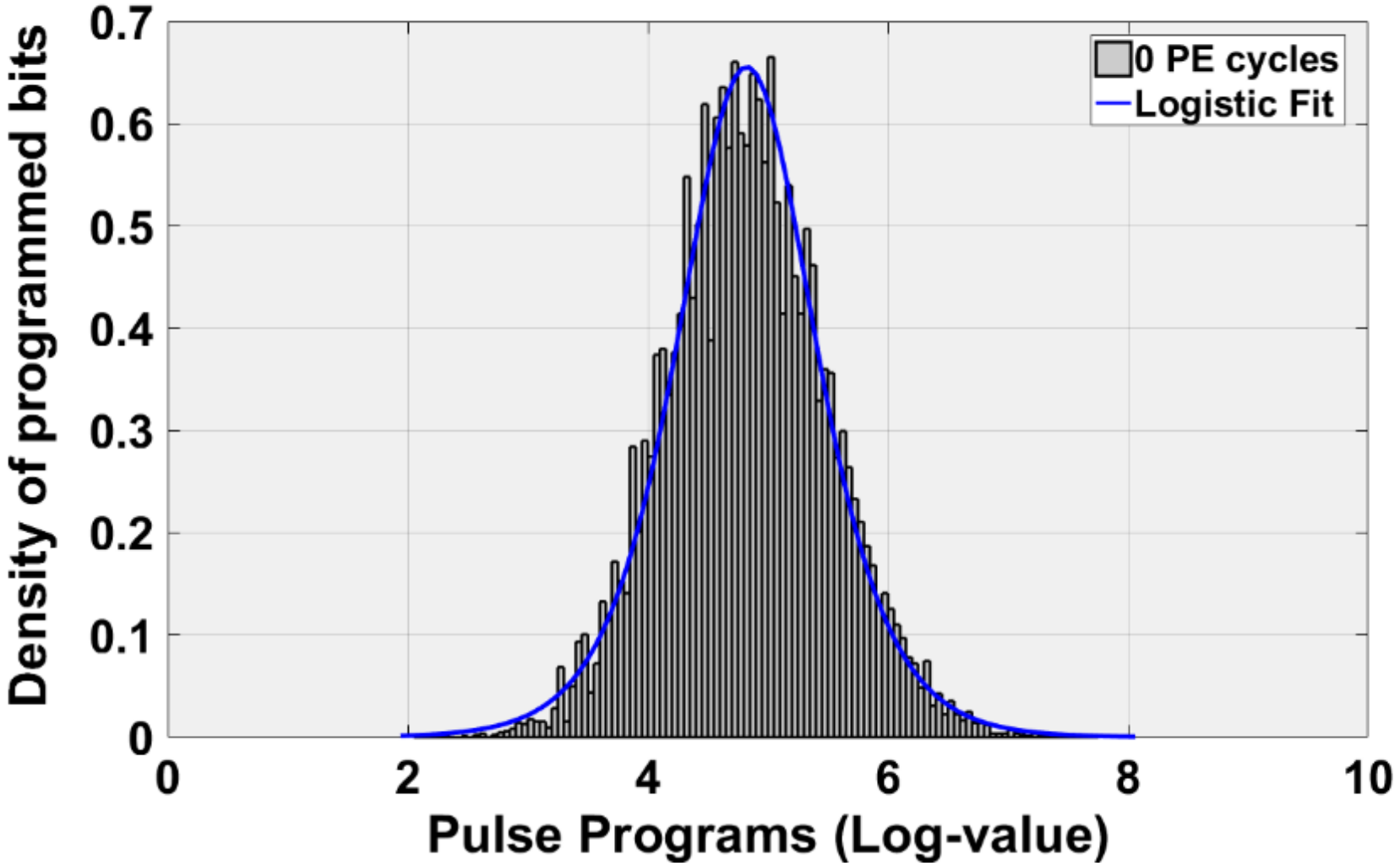


Coupled effect of Radiation and Endurance

The endurance stress gradually shifts the curve for different TID levels.
Data retention studies can throw some light on the reliability of the such a block.



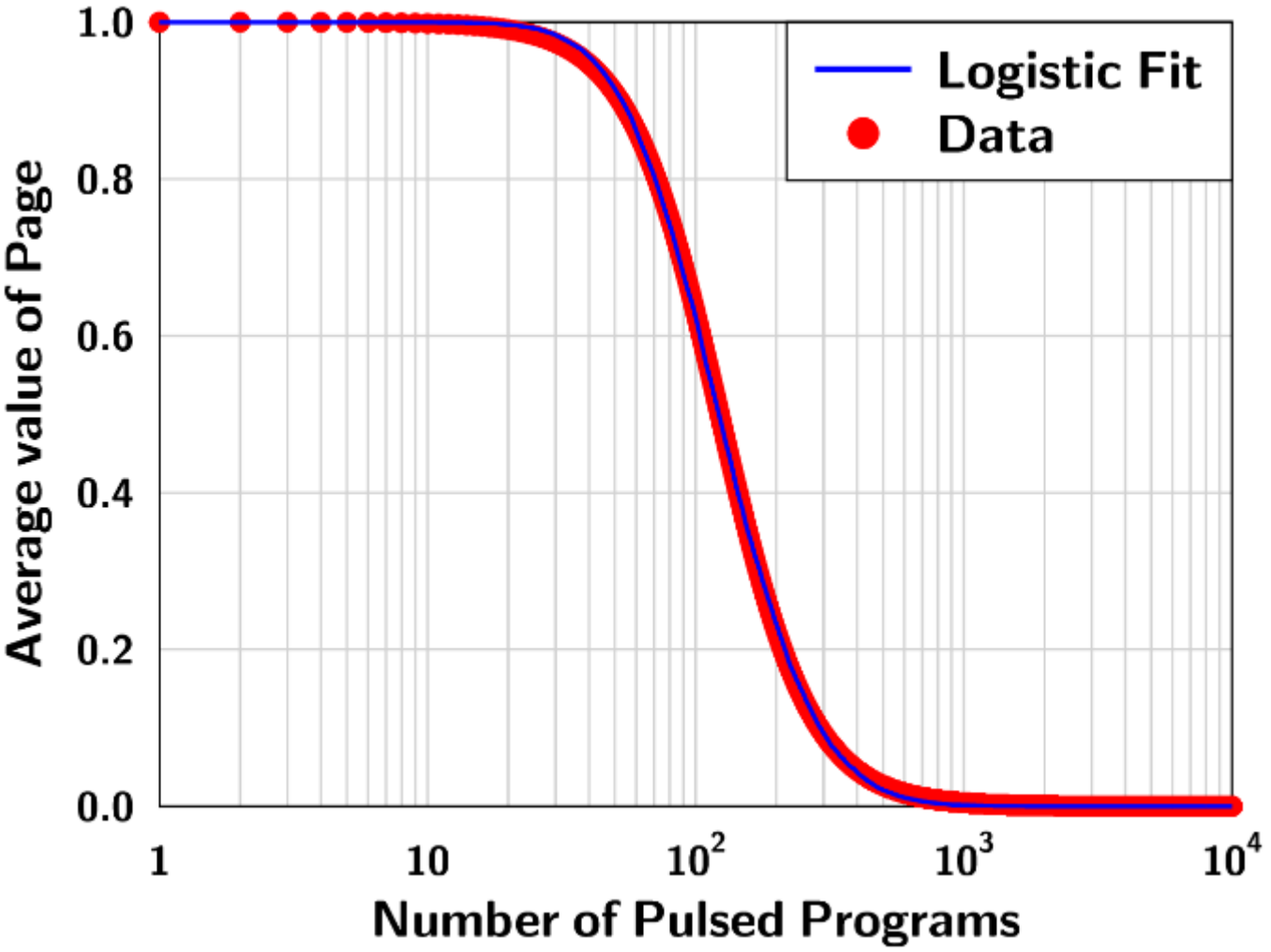
Bit distribution and statistical models



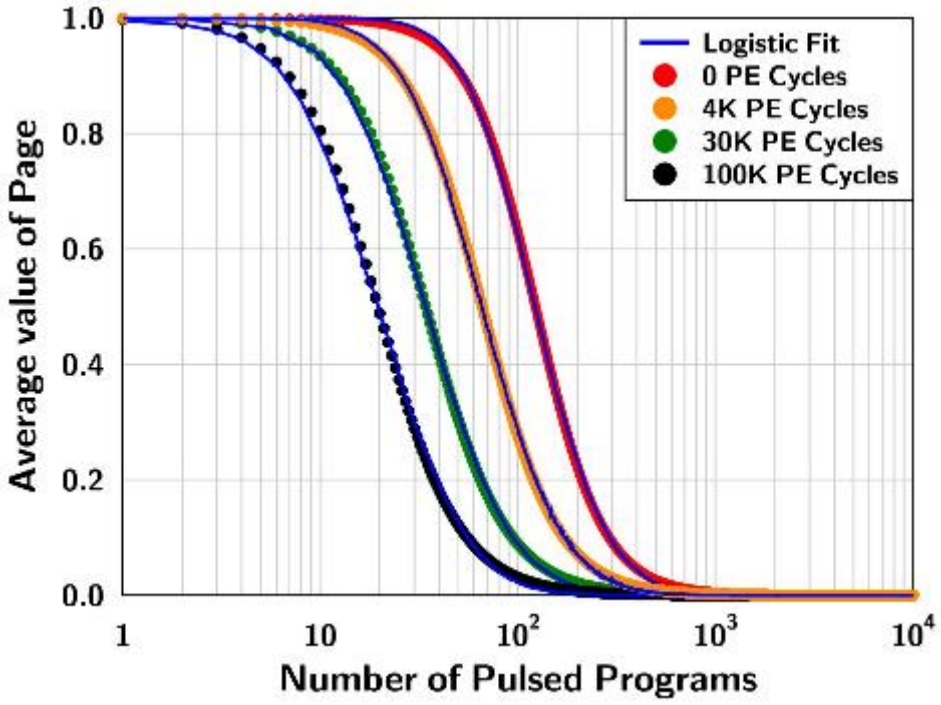
Fitting to a Logistic model

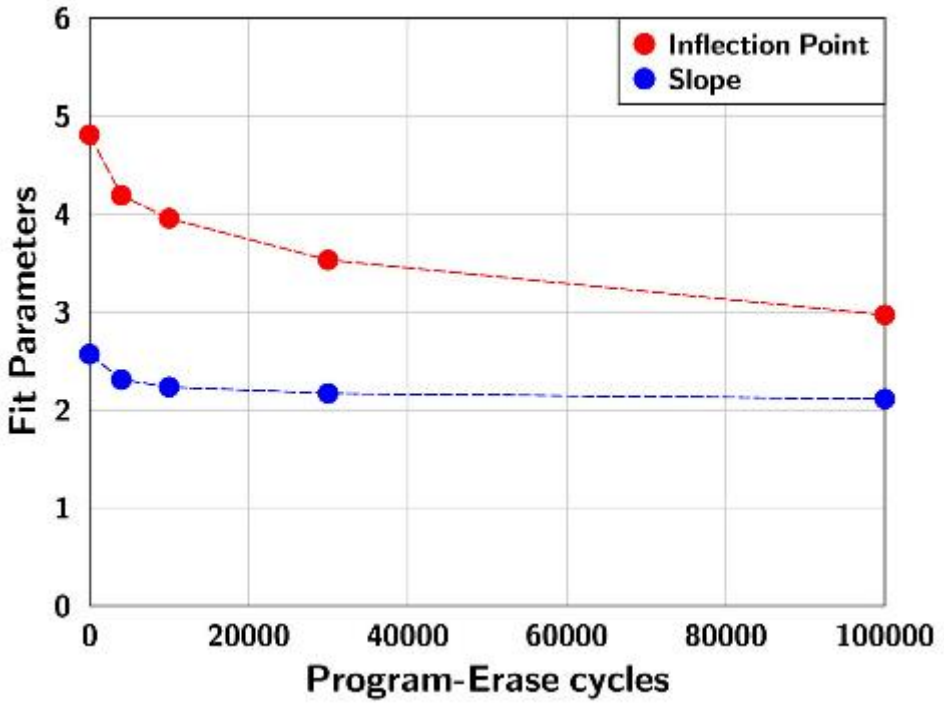
$$y = \frac{1}{1 + e^{a(x-b)}}$$

a: Slope
b: Inflection point
y: Avg. value
x: Pulsed Program



Fit Parameters and PE Cycles





Slope does not change much in comparison to inflection point

Neutral Trap Model

- **Post-Radiation PE cycling is studied largely**
- **We study Pre-radiation PE cycling which show similar results.**
- **We believe the trap state location is the key**

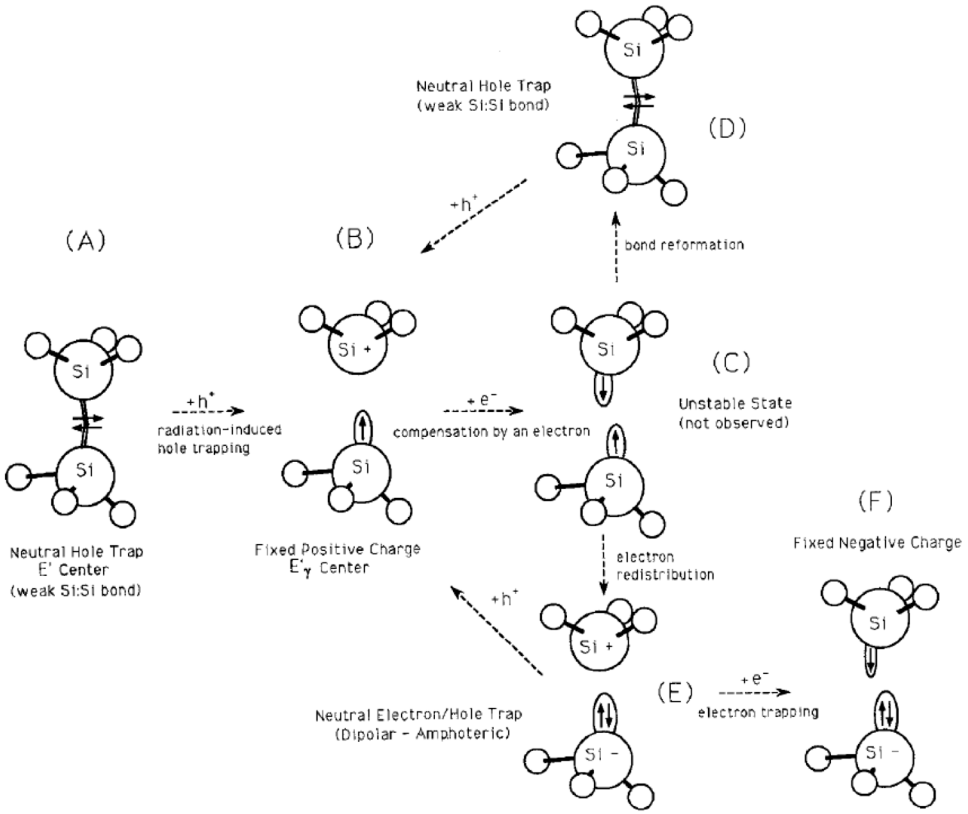


Figure taken from J. Electrochem. Soc.-1991-Walters-2756-62

Conclusions and Remarks

- **Pulsed programming provides a chip level test to evaluate the programming speed and thus the trap states**
- **Logistic model is an appropriate model to mathematically fit the program pulse data as well as bit distribution data**
- **Data was successfully retained on a chip for 3 weeks at 100 ^{o}C**
- **Activation energies and physical-parameter correlation of bit distribution is necessary and on-going.**

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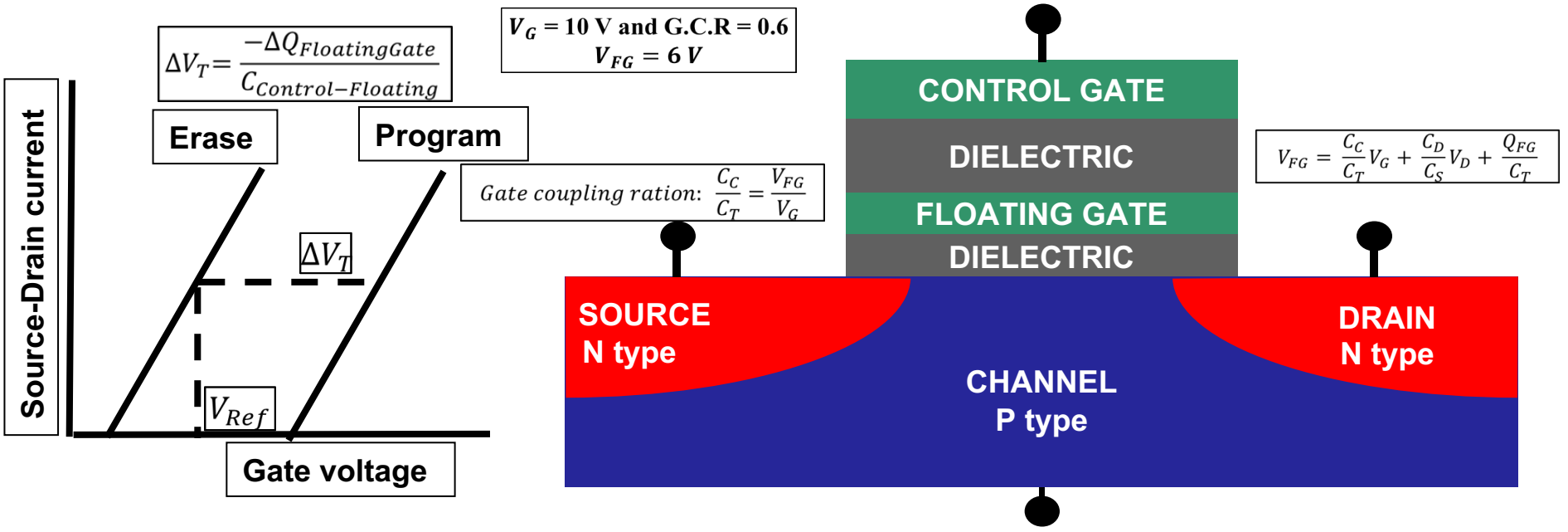
Back up slides

Basics of Floating gate device

Large **positive** (**negative**) bias on the control gate **induces** (**extracts**) electrons in (from) the floating gate.



The **presence** or **absence** of electrons on the floating gate controls the **source-drain current** and bit is either **programmed "0"** state or **erased "1"**

Storing charge in floating gate or tunneling

A large positive bias bends the barrier towards the gate and the probability of tunneling of electrons increases thus electrons are stored in the floating gate.